IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

XMTT, INC., Plaintiff, v. INTEL CORPORATION, Defendant.	Civil Action No. 1:18-cv-01810-MFK **REDACTED - PUBLIC VERSION**

OPENING BRIEF IN SUPPORT OF INTEL'S
MOTION FOR SUMMARY JUDGMENT AND
MOTION TO EXCLUDE OPINIONS OF PLAINTIFF'S EXPERTS

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INTRODUCTION

"Parallel" processing is ***not*** "serial" processing, and parallel processors are ***not*** serial processors. The patents-in-suit rely on that distinction. As XMTT itself has put it, "[t]he system in the '388 patent comprises a serial processor and functionally non-equivalent parallel processors." Ex. 1 at 9. XMTT's expert agreed, stating that the patent "uses a system in which the serial processors are specialists designed to perform serial computing and the parallel processors are specialists designed to perform parallel computing." Ex. 2 ¶69; *see also* Ex. 3 ¶23.

Every asserted claim requires a "serial processor [] to execute [] instructions . . . primarily in serial" or a system operating in "serial processing mode." Under the plain meanings of those terms, XMTT must show that the accused products contain a processor that executes instructions serially: one at a time, in a sequential manner—*i.e.*, not in parallel. XMTT cannot meet that burden because the accused Intel products contain ***only*** parallel processors. There is no factual dispute that the accused Intel products are multi-core central processing units (CPUs) in which the cores execute multiple threads of instructions concurrently in parallel with each other, and each core itself issues and executes multiple instructions simultaneously in parallel, as they are designed to do. Accordingly, XMTT cannot prove that any accused product literally meets the "serial processor" or "serial processing mode" limitations of the asserted claims.

XMTT's doctrine of equivalents theory fares no better. The asserted claims require ***both*** a "serial" processor and "parallel" processors. XMTT's attempt to equate serial and parallel processors erases the patents' clear distinctions between those terms, thereby vitiating the "serial processor" claim element. Moreover, because a "serial" processor is the opposite of a "parallel" processor, the two cannot be equivalent under the law. The undisputed evidence shows that Intel's highly parallelized cores are substantially different from a specialist serial processor that executes instructions one at a time. In fact, on more than one occasion prior to this lawsuit, the inventor,

Dr. Vishkin, drew a "sharp contrast" between the approach described in XMTT's patents and Intel's graphics processing unit (GPU) approach, as used in the accused products. The Court should thus grant summary judgment of non-infringement on all claims.

XMTT also cannot show that Intel had the requisite knowledge of either the patents or of infringement to sustain a pre-suit willfulness claim. Dr. Uzi Vishkin has admitted that prior to filing this lawsuit, neither he nor XMTT ***ever*** notified Intel of the patents or of a belief that Intel infringed, and there is no evidence contradicting Dr. Vishkin's testimony or showing that Intel had knowledge. Thus, the Court should grant summary judgment of no pre-suit willful infringement.

In addition, XMTT's damages demands rest on flawed and unreliable expert testimony. First, XMTT intends to ask the jury for [redacted] based on the analysis of its damages expert, Dr. Ryan Sullivan, who offers wildly varying damages theories. Dr. Sullivan splits his theories into two categories, an "income approach" and a "market approach." Dr. Sullivan bases his income approach on a fatally defective regression analysis and relies upon the value of conventional components rather than value attributable to the claimed invention. Dr. Sullivan also violates established law by awarding XMTT 100% of Intel's incremental profits. Accordingly, the Court should exclude Dr. Sullivan's income approach from presentation at trial.

Second, the technical opinions that support Dr. Sullivan's income approach are also flawed. In particular, Dr. Murali Annavaram, who conducted graphics "performance" testing, offers opinions entirely divorced from the evidence and his own testing results. Dr. Annavaram disabled components in the accused processors and tested the associated "performance" drop using a gaming benchmark. He then claimed that the performance benefits conferred by the patents are equivalent to the hypothetical addition of more processor execution units ("EUs"). But Dr. Annavaram's assumption of "equivalence" is unsupported by any evidence and is inconsistent

with both the single Intel document Dr. Annavaram cites and the results of his own testing. Furthermore, Dr. Annavaram illogically measures the impact of removing two different components—one for each patent—even though XMTT says removing one constitutes a non-infringing alternative for both patents-in-suit. Accordingly, the Court should exclude Dr. Annavaram's performance improvement opinions and the damages estimates based thereon.

NATURE AND STAGE OF THE PROCEEDINGS

XMTT filed this action on November 16, 2018, alleging that Intel infringes two closely related patents—U.S. Patents 7,707,388 ("'388 patent") and 8,145,879 ("'879 patent"). D.I. 1. Trial is currently set for April 24, 2023. D.I. 256.

SUMMARY OF THE ARGUMENT

1. There is no genuine dispute about how any of the accused Intel products work, and based on the undisputed facts XMTT cannot prove that the "serial processor" or "serial processing mode" elements of the asserted claims are literally met. The accused products contain ***only*** parallel processors. *First*, the accused products are multi-core CPUs, in which each core is designed to execute instructions concurrently in parallel with the other cores. *Second*, each core is a multiple-issue processor that issues and executes multiple instructions at the same time in parallel. And *third*, many of the accused products use Hyper-Threading, a technique that allows each core to simultaneously execute two streams of instructions in parallel. Accordingly, no accused product has the claimed "serial processor." XMTT seeks to avoid these undisputed facts by focusing its infringement analysis on the order in which instructions are written in programs and the order in which Intel's cores "retire" instructions after execution. But XMTT has no evidence that any of the accused processors ***executes instructions*** primarily in serial—*i.e.*, one at a time, in a sequential manner (and without a serial processor, the products likewise lack a serial processing mode). Accordingly, the accused products are missing a claim element of every asserted claim, and as a

matter of law, XMTT cannot prove literal infringement.

2. XMTT also cannot prove infringement under the doctrine of equivalents because, contrary to XMTT's assertion, the highly parallelized cores in the accused Intel products are not equivalent to serial processors. Under the vitiation doctrine, XMTT's doctrine of equivalents theory must fail because it would entirely eliminate the "serial processor" limitation, and erase all distinction between it and the separately claimed "plurality of parallel processors." Moreover, the plain language of the claims, the specifications of the patents, and myriad extrinsic evidence demonstrate that "serial" and "parallel" processors are antithetical to each other. Thus, under the "specific exclusion" principle, these two opposites cannot be equivalent as a matter of law. At bottom, the undisputed evidence demonstrates that Intel has designed its products to be parallel processors that execute multiple instructions in parallel, using substantial amounts of sophisticated hardware dedicated to parallel execution—all of which makes the accused products, and their cores, substantially different in kind from the claimed serial processor. And Intel's multi-core processors perform a different function (execution of instructions in parallel) in a different way (employing parallelism at all stages of processing) to achieve different results (improved performance) than a serial processor. Accordingly, the Court should grant summary judgment because XMTT cannot prove infringement under the doctrine of equivalents as a matter of law.

3. Based on the undisputed facts, XMTT cannot meet its burden to prove willful infringement by showing that Intel had knowledge of, or was willfully blind to, the asserted patents or infringement. Dr. Vishkin testified that prior to filing this lawsuit, neither he nor XMTT ever notified Intel of the '388 and '879 patents or a belief that Intel was infringing. XMTT relies on a history of communications between Dr. Vishkin and people within Intel, but not a single piece of evidence contradicts Dr. Vishkin's own testimony or shows that he ever mentioned the '388 or

'879 patent to any person at Intel. And the undisputed evidence shows that Dr. Vishkin spent years attempting to persuade Intel to adopt his technology and criticizing Intel's technology as "broken" and "sub-optimal," but Intel continued on its own path rather than using Dr. Vishkin's approach. The Court should therefore grant summary judgment of no pre-suit willful infringement.

4. Dr. Sullivan should be precluded from presenting his flawed "income approach" to damages at trial. Dr. Sullivan purports to determine a statistical correlation between the price of the accused products and the number of EUs that the accused processors contain, but he treats that claimed correlation as causation, calculating a supposed 'price benefit' to Intel resulting from additional EUs—without any evidence whatsoever that additional EUs themselves cause the alleged price increases. His underlying statistical analysis is fatally defective and exacerbates the correlation-does-not-equal-causation problem. *First*, Dr. Sullivan's income-approach regression model suffers from at least two critical design flaws: he treats his "parameter of interest," EUs, as a continuous variable though that physical unit cannot exist in fractional form; and he ignores the strong correlation between EUs and other variables that disrupts his model's explanatory power. Together, these flaws make it impossible for Dr. Sullivan's regression model to isolate either the precise correlation on which he relies, or the value of the patented technology. *Second*, Dr. Sullivan's damages calculations rely on inputs from XMTT's technical experts that ostensibly quantify the benefits of the patented invention relative to what they identify as the closest non-infringing alternative for each patent. But the technical experts improperly focused on the impact of ***conventional*** components of the claims, whereas the law requires that damages be tied to the patents' alleged improvement over the prior art. *Third*, even if Dr. Sullivan were able to determine incremental revenue from his regression model, he improperly awards XMTT 100% of Intel's incremental profits. Because he fails to consider Intel's bargaining position at the

hypothetical negotiation, Dr. Sullivan's "profit split" has no basis in fact and is contrary to law.

5. The Court should also preclude Dr. Annavaram, XMTT's system testing expert, from presenting his assessment of graphics performance enabled by the patented technology. First, Dr. Annavaram conducted graphics performance tests to quantify performance improvements that he attributes to the patented technology, then he attempted to convert those performance improvements into what he calls an "equivalent hardware change," *i.e.*, an increase in EUs, for use in Dr. Sullivan's analysis. But the evidentiary basis for the conversion is nonexistent. Dr. Annavaram's only alleged support is his arbitrary comparisons of pairs of computer systems in a single Intel document that used different measurements and which showed that graphics performance and the number of EUs are not equivalent—a fact that Dr. Annavaram attempts to gloss over by calling his opinion "conservative." Second, Dr. Annavaram's opinion unaccountably adds the impact of removing two components, even though XMTT concedes that removing a single component would result in non-infringement of both patents.

STATEMENT OF THE FACTS

A. XMTT's Patents Are Directed To Computer Systems With A "Serial Processor" That Executes Instructions Primarily In Serial And Operate In A "Serial Processing Mode"

Both asserted patents are directed to a "Computer Memory Architecture for Hybrid Serial and Parallel Computing Systems" intended to allow "efficient computation of serial processing, parallel processing or any mix of the two including primarily serial computing, or primarily parallel computing," and support "seamless transitions between parallel and serial processing modes." Ex. 4 at 1:25-27, 1:61-65; Ex. 5, 1:32-34; 2:1-5. Each of the asserted claims[1] requires (1) a "serial processor to execute instructions in a computing program primarily in serial"; (2) a

[1] XMTT asserts the following claims: '388 patent, claims 1, 4, 13, 14, 16, 18, 19, 21, 22, 26, 31, and 33; and '879 patent, claims 1, 4, 7, 15, 20, 23, 25, and 26. Ex. 6, ¶84.

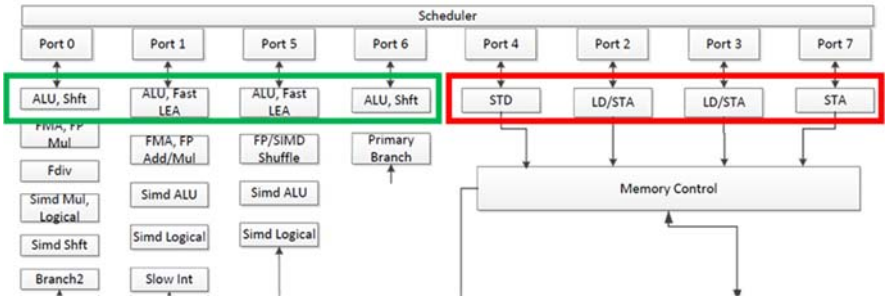
"serial processor adapted to execute software instructions in a software program primarily in serial"; (3) a "serial processing mode"; or some combination thereof. Ex. 4, claims 1, 19, 33; Ex. 5, claims 1, 20. The asserted claims also require, by contrast, "parallel processors" that execute instructions in parallel and a "parallel processing mode." *Id*.

B. XMTT Accuses Intel's Multi-Core Processors Of Meeting The "Serial Processor" And "Serial Processing Mode" Limitations—Even Though They Are Parallel Processors That Execute Multiple Instructions In Parallel

In this case, XMTT accuses Intel's multi-core CPUs with integrated GPUs of infringement. D.I. 1 ¶15, 43; Ex. 6 ¶¶87-90. XMTT contends that each accused product has a core that is a "serial processor" that executes instructions primarily in serial. Ex. 6 ¶172.

Intel's multi-core CPUs contain multiple cores, each of which executes instructions concurrently and in parallel with the other cores and with the integrated graphics processors. Ex. 7 ¶23; Ex. 8 ¶10; Ex. 9 ¶15; Ex. 10 at 102:23-103:23. Moreover, each core itself employs "multiple-issue" parallel processing techniques to issue and execute multiple instructions in parallel using parallel functional units. Ex. 7 ¶¶9, 12; Ex. 8 ¶5 & n.1; Ex. 9 ¶¶8-9; Ex. 10 at 109:5-15; 112:7-16; 113:13-16; 125:13-19.

The accused "Haswell" products, for example, have between two and eighteen cores that operate concurrently in parallel with each other to execute instructions. Ex. 7 ¶23. And each Haswell core uses multiple-issue parallel processing to simultaneously issue up to eight instructions for parallel execution. *Id*. ¶¶12-13. As shown below, the Haswell core can execute four arithmetic instructions (*e.g.*, adding two numbers together, in green below) and four load/store instructions (*e.g.*, storing data in memory, in red below) simultaneously in parallel, because it has four arithmetic logic units and four load/store units in the instruction execution stage:



Ex. 7 ¶12 (red & green annotations added); *see also* Ex. 43 (identifying the "instruction execution stage"); Ex. 10 at 161:22-162:1. All of the accused cores similarly function by simultaneously issuing multiple instructions for parallel execution. Ex. 7 ¶¶9, 12; Ex. 8 ¶5 & n.1; Ex. 9 ¶¶8-9. And most accused products support Hyper-Threading™, Intel's name for the parallel processing technique of "simultaneous multi-threading," which further enables each core to execute two different threads—streams of instructions—in parallel, effectively creating two virtual cores for each physical core in the processor. Ex. 7 ¶¶21-22; Ex. 8 ¶8. None of the accused cores executes instructions in a sequential manner, one at a time. Ex. 7 ¶25; Ex. 8 ¶15; Ex. 9 ¶20.

C. Although Dr. Vishkin Contacted Intel Repeatedly, Neither He Nor XMTT Notified Intel Of The Asserted Patents Or The Alleged Infringement Before Filing This Lawsuit

Before filing this lawsuit, Dr. Vishkin—XMTT's sole employee—repeatedly urged Intel to adopt his "XMT" technology. Although Intel declined to do so, XMTT now contends that Intel willfully infringes the asserted patents based on Dr. Vishkin's unsuccessful campaign. Ex. 6 ¶¶541-43.

In fact, Dr. Vishkin never notified Intel of the asserted patents before filing this lawsuit, nor did he ever communicate a belief that the accused Intel products—multi-core CPUs with integrated GPUs—infringed the asserted patents. Ex. 11 at 39:18-22, 96:3-13. Dr. Vishkin only referred to a patent application ("US patent application 20090119481") which he described in "sharp contrast" to the GPU approach that XMTT now accuses of infringement. Ex. 13 at 1; Ex.

14 at 1, 4. And XMTT has identified no evidence that Intel otherwise acquired knowledge of the '388 or '879 patents.

Moreover, after the asserted patents issued, Dr. Vishkin repeatedly criticized Intel's processors (calling them "broken" and "highly suboptimal") to try to convince Intel to abandon its architecture and adopt his approach. Ex. 15 at 1; Ex. 16 at 2; Ex. 12 at 362:3-363:2. Intel did not; instead, it stuck with its own architecture and designs—yet XMTT now accuses the same products Dr. Vishkin told Intel were broken because they did not use his XMT approach.

D. Dr. Sullivan's Flawed Income Approach

Dr. Sullivan provides an "income approach" in his report, which attempts to estimate the additional income Intel earned by selling processors with the accused technology. Ex. 17 ¶¶187-89. In that analysis, Dr. Sullivan designed a regression model that includes Intel sales information and many of its processors' features, which purportedly identifies a correlation between the price of each processor and its number of EUs; he then uses that correlation to assert causation of price benefits stemming from additional EUs. *Id.* ¶21. However, Dr. Sullivan treats EUs as a ***continuous*** variable that can increase by a percentage amount (instead of a discrete variable that can only increase by integers), *id.* ¶¶249, 251, and does not account for the fact that each execution ***unit*** is [redacted] Ex. 6 ¶¶136-37, 219. Dr. Sullivan also does not account for multiple strong correlations between EUs and other processor features, which means that his supposed correlation between EUs and price is tainted with the value of other features.

XMTT recognizes that EUs are not the claimed invention, but XMTT's technical experts contend that the alleged infringement results in either "die area savings" or graphics "performance improvement" benefits that can be equated to additional EUs. Both of XMTT's experts focus on the same components: an L3 graphics cache (allegedly the claimed "partitioned memory

modules") for the '388 patent and an L2 sampler cache (allegedly the claimed "read-only memory") for the '879 patent. *See* Ex. 6 ¶¶443-44; Ex. 10 at 108:3-6, 17-20; Ex. 18 ¶¶37-38, 44. Those components, however, are conventional technology that was well-known in the art—Drs. Vishkin and Conte both ***admit*** that the graphics L3 cache and the L2 sampler cache are ***conventional*** elements of the asserted claims. Ex. 11 at 159:5-160:13, 165:6-13; Ex. 19 ¶¶780, 782, 786, 789; Ex. 10 at 51:4-11, 63:25-64:10, 201:9-17. In fact, Dr. Annavaram—who identified the components—admitted that he did not even review the prior art before deciding which components to test. Ex. 20 at 249:20-250:2, 251:2-9, 253:11-18, 258:13-20; 264:23-265:9.

Using the input from XMTT's technical experts, Dr. Sullivan assumes that the hypothetical "additional" EUs can be translated into additional income (via the correlation provided by his regression model) that he claims Intel realized through infringement. Ex. 17 ¶¶283, 288-99. Dr. Sullivan splits that hypothetical additional income per processor between Intel and XMTT by deducting [redacted] "returning" to Intel its sales and marketing, general and administrative, and research and development costs, and awarding the remainder—the ***entire profit*** purportedly derived from the patented technology—as a royalty to XMTT. *Id.* ¶¶303, 316-24, 330-35 & Attachments I-1, K-1. In effect, Dr. Sullivan assumes Intel should receive nothing more than it would have obtained if it had sold the accused products without the alleged invention.

E. Dr. Annavaram's Valuation of Graphics Performance Opinions

Dr. Annavaram purports to measure the performance improvement due to the alleged invention by measuring differences in graphics performance with the L3 graphics cache (allegedly "partitioned memory modules") and the L2 sampler cache (allegedly "read-only memory") in the accused products enabled and disabled. First, Dr. Annavaram took fifteen computer systems with the accused processors and modified them to disable the L3 graphics cache and L2 sampler cache. Ex. 18 ¶¶33, 51. He then ran a gaming benchmark called Unigine Heaven to test the frames-per-

second (FPS) rate on the fifteen systems in their normal state as well as in their "non-infringing" state, *i.e.*, with disabled caches. *Id.* ¶¶20, 51, 53. Dr. Annavaram then used those FPS measurements to calculate performance differentials ostensibly attributable to the disabled components, though without consistent results across the various computer systems. *Id.* ¶56. Dr. Annavaram then discarded the results from fourteen of the tested systems and selected the results from ***one*** computer system—the xmtt-OptiPlex-9020 system which had "the lowest-combined benefit" of "9.63%, comprised of a 5.30% benefit for the '879 patent and a 4.33% benefit for the '388 patent"—as a supposed "conservative representative of the benefit of the patents to all the accused systems." *Id.* ¶57. In fact, however, several systems had significantly lower benefits on a per-patent basis: *e.g.*, xmtt-macbook12, xmtt-MacBookAir, and xmtt-Latitude-E5450 for the '879 patent, and xmtt-b75m-d3p and xmtt-latitude-e6530 for the '388 patent. *Id.* ¶56.

For Dr. Sullivan to use his results, Dr. Annavaram needed to translate his supposed "performance improvement" into EUs. He did so by assuming that an "[i]ncrease in graphics performance can be attributed to an equivalent increase in the number of execution units on a given computing system." *Id.* ¶¶59-62. Dr. Annavaram bases that claimed equivalence, not on his testing, but on performance results from a ***different*** metric using a ***different*** gaming benchmark—namely, 3DMark Performance Graphics Score—contained in [redacted]. *Id.* ¶60; Ex. 21. Dr. Annavaram identified results from [redacted] (Ex. 21)—and "[redacted]." Ex. 18 ¶61. Based on those calculations—which did not show any consistent relationship, Ex. 20, 214:19-215:12, 216:13-24—he concluded that [redacted]." *Id.* Dr. Annavaram then jumps from that analysis to his conclusion

that [redacted] (*id.* ¶62)—ultimately concluding that the patents-in-suit allow [redacted]. *Id.* ¶57; Ex. 17 ¶¶282, 291, 297.

ARGUMENT[2]

I. THE COURT SHOULD GRANT SUMMARY JUDGMENT OF NONINFRINGEMENT

XMTT cannot show that Intel infringes any asserted claim, because none of the accused Intel products contains a "serial processor" that executes instructions in serial or operates in a "serial processing mode" as the asserted claims require. The Court should thus grant summary judgement of noninfringement on all asserted claims.

A. The asserted claims require a serial processor that executes instructions in serial—i.e. one at a time, in a sequential matter

Every asserted claim requires a "serial processor" that executes instructions in a program primarily in serial or a "serial processing mode." Ex. 4, claims 1, 19, 33; Ex. 5, claims 1, 20. The Court has not construed either term, thus they are governed by the ordinary and customary meaning. *See, e.g.*, *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). And the evidence allows no dispute that the ordinary meaning of a serial processor that executes instructions in serial is a processor that executes instructions one at a time, in a sequential manner.

XMTT's patents and Dr. Vishkin's contemporaneous admissions demonstrate that a serial processor executes one instruction at a time in a sequential manner. The asserted patents describe serial execution as using a "von Neumann or other sequential architecture." Ex. 4 at 4:39-42.

[2] Intel incorporates the Court's legal standards for summary judgment and *Daubert* motions in *Plastic Omnium Advanced Innovation & Research v. Donghee America, Inc.*, 387 F. Supp. 3d 404, 409-11 (D. Del. 2018).

Dr. Vishkin, in other contemporaneous patents (including the '527 patent, which appears on the face of the patents-in-suit), confirmed that in a "so-called 'von-Neumann architecture,' … each instruction of the program is then executed sequentially" (Ex. 22 at 1:12-17; *see also* Ex. 23 at 1:38-46), and that "processing follows a set of sequentially executed instructions, without any concurrent operations." Ex. 24 at 1:21-28. Moreover, Dr. Vishkin also describes a "serial order of execution" as one "where only one instruction is scheduled for execution at a time." Ex. 22 at 1:38-40; Ex. 23 at 1:38-46. Similarly, XMTT itself has conceded that a "serial processing mode" is a mode in which the system is executing in serial. D.I. 224 at 22-23. XMTT and its experts have admitted that the patents require a "specialist" serial processor, specifically designed to operate primarily in serial, and which is "functionally non-equivalent" to a parallel processor. Ex. 1 at 9; Ex. 2 ¶69; Ex. 3 ¶23. Dr. Vishkin himself has confirmed those admissions. Ex. 12 at 505:8-507:24, 513:5-18.

Additionally, the evidence allows no genuine dispute that a parallel processor executing instructions in parallel, *i.e.* executing multiple instructions concurrently, cannot be the claimed serial processor. The asserted claims require ***both*** a "serial processor" and "parallel processors" to be present, Ex. 4, claims 1, 19, 33; Ex. 5, claims 1, 20, which confirms that, as a matter of law, the two types of processors are different. *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008) ("different claim terms are presumed to have different meanings"). And the specifications consistently contrast "serial" and "parallel" processors (Ex. 4 at 4:39-46) as do technical dictionaries from the time of the patents (Exs. 25; 26; 27; 28) and other patents and publications from Dr. Vishkin (Ex. 23 at 7:40-49; Ex. 29 at 2; Ex. 30 at 1; Ex. 31 at 2-3) as well as his testimony on behalf of XMTT. Ex. 12 at 358:4-15.

B. No genuine dispute exists that the accused products execute instructions in parallel—they are not serial processors that execute instructions one at a time in a sequential manner

The operation of the accused Intel products is not disputed—they always ***execute*** instructions in parallel in multiple fashions, not one at a time in a sequential manner.

1. The accused Intel products have multiple cores that execute instructions in parallel with each other

First, no dispute exists that the accused Intel products are multi-core parallel processors. Ex. 7 ¶23; Ex. 8 ¶10; Ex. 9 ¶15; Ex. 10 at 102:23-103:33; Ex. 12 at 460:21-24; Ex. 32, Exhibit A ¶¶92-94, 126, 227-33. Each accused Intel product has between two and forty cores, and those cores execute multiple threads of instructions concurrently in parallel with each other. Ex. 7 ¶23; Ex. 8 ¶10; Ex. 9 ¶15; Ex. 32, Exhibit A ¶228.

XMTT concedes that multi-core processors are parallel processors, rather than serial processors. At his 30(b)(6) deposition, Dr. Vishkin conceded that [redacted] and has described multi-core processors as parallel processors in his publications. Ex. 12 at 455:15-456:7, 460:21-461:6; Ex. 30 at 3. Similarly, Dr. Conte, XMTT's infringement expert, admits that "a multi-core CPU is designed to execute software instructions at the same time (***in parallel***) in more than one core" and that, in multi-core processors, a "software program can be broken down into independent blocks or 'threads' and executed across the multiple cores in order to ***allow fast, parallel processing***." Ex. 33 (emphasis altered from original); Ex. 10 at 166:3-8, 171:7-15; *see also* Ex. 34 at 2.

2. Each core in the accused Intel products issues and executes instructions in parallel, not in serial

Second, no dispute exists that each core in the accused Intel products is a multiple-issue processor that issues and executes multiple instructions in parallel. Ex. 7 ¶¶11-13; Ex. 8 ¶5; Ex. 9 ¶¶7-9; Ex. 10 at 113:13-16. Each core includes multiple decoders that process multiple

instructions in parallel, decoding each into one or more "micro-operations." Ex. 7 ¶¶ 9 & n.3, 15; Ex. 8 ¶¶ 5 & n.1, 6; Ex. 9 ¶¶10-11; Ex. 32, Exhibit A ¶¶205-08, 216. Micro-operations are themselves "very simple instructions." Ex. 35 at 89, 138; *see also* Ex. 10 at 112:7-16. Each core has schedulers that issue multiple micro-operations (up to ten in the latest Intel processors) for execution at once. Ex. 7 ¶¶11-13, 15; Ex. 8 ¶5; Ex. 9 ¶¶7-9; Ex. 32, Exhibit A ¶¶205-08. Then, during execution, multiple execution units (arithmetic logic units, load/store units, multipliers, etc.) within each core execute those simple instructions in parallel. Ex. 7 ¶¶11-13; Ex. 8 ¶5; Ex. 9 ¶¶7-9; Ex. 32, Exhibit A ¶¶205-08.

XMTT does not dispute that the accused processors are multiple-issue processors that execute instructions in parallel. Ex. 10 at 113:13-16. Moreover, Dr. Vishkin admitted that a [redacted]:

Q [redacted].

Ex. 11 at 154:5-9 (objection omitted). XMTT's expert, Dr. Conte, similarly admits that the accused cores [redacted] Ex. 10 at 126:22-127:1, 145:5-11. And Dr. Conte concedes that, even though [redacted]. *Id.* at 143:10-19, 147:7-17.

3. The cores in many of the accused Intel products use simultaneous multi-threading to execute instructions from two threads in parallel

Third, no dispute exists that each core in the "big Core" Intel products[3] executes two

[3] The accused "big Core" products are Ivy Bridge, Haswell, Broadwell, Crystal Well, Skylake, Kaby Lake, Coffee Lake, Whiskey Lake, Amber Lake, Comet Lake, Ice Lake, Tiger Lake, and Rocket Lake. Ex. 32, Exhibit A ¶86. XMTT identified Alder Lake products as allegedly infringing for the first time in its expert reports. *Id.*, Exhibit A ¶86, n.17; Ex. 6 ¶164. Intel disputes that Alder Lake products are properly accused or at issue within this case.

threads in parallel using Intel's Hyper-Threading™ technology, an implementation of simultaneous multi-threading. Ex. 7 ¶¶21-22; Ex. 8 ¶8; Ex. 32, Exhibit A ¶¶237-39. Hyper-Threading allows a multiple-issue processor to execute multiple instructions in parallel from two threads of instructions, not just one thread of instructions (Ex. 7 ¶¶21-22; Ex. 8 ¶8; Ex. 32, Exhibit A ¶¶237-239), thus further increasing the parallelism in Intel's processors by effectively doubling the number of virtual cores for each physical core.

XMTT does not dispute that ***each core*** in the accused Intel "big Core" products simultaneously executes two threads—two streams of instructions—in parallel. Again, Dr. Vishkin admitted that [redacted]

Ex. 11 at 149:6-9. XMTT's experts agree. Ex. 10 at 126:2-10; Ex. 20 at 108:6-20.

C. The accused Intel processors do not literally infringe the asserted claims because they have neither serial processors nor a serial mode—the accused cores are parallel processors that execute instructions in parallel

XMTT has the burden to prove infringement by showing that the accused products contain every claim element, including the "serial processor" and "serial processing mode" elements. *Kahn v. Gen. Motors Corp.*, 135 F.3d 1472, 1477 (Fed. Cir. 1998). Under the plain meanings of those terms, XMTT must show that the accused products contain a processor that executes instructions one at a time, in a sequential manner. *See* Section I.A, *supra*. But it is undisputed that the cores in the accused products execute multiple threads of instructions concurrently in parallel with each other, and that each core issues and executes multiple instructions simultaneously in parallel. *See* Section I.B, *supra*. Thus, no "reasonable jury" could find that the accused products contain a serial processor or operate in a serial processing mode. *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986).

XMTT's expert, Dr. Conte, asserts that the [redacted] (Ex. 10 at 140:9-141:10); but that assertion is insufficient to prove infringement for two reasons. First, the language of the claims requires a "serial processor" "to ***execute*** software instructions . . . primarily in serial." Ex. 4, claims 1, 19, 33; Ex. 5, claims 1, 20. Thus, Dr. Conte's analysis, which focuses on [redacted]. 10 at 141:1-22, 143:10-19), fails to account for the actual claim language and has no weight. *See Huawei Techs., Co, Ltd v. Samsung Elecs. Co, Ltd.*, 340 F. Supp. 3d 934, 967-68 (N.D. Cal. 2018) (striking expert opinions which were "improperly based on claim construction arguments" contrary to term's plain meaning); *see also Applied Signal Tech., Inc. v. Emerging Markets Commc'ns, Inc.*, No. C 09-2180, 2011 WL 500786, at *3 (N.D. Cal. Feb. 9, 2011) (holding that the court may "not accord weight to expert testimony which contradicts the clear language of the claim" (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584 (Fed. Cir. 1996))). Second, Dr. Conte's assertion disregards the undisputed fact that the cores retire multiple instructions in a single cycle in parallel. Ex. 7 ¶¶14-16; Ex. 8 ¶6; Ex. 9 ¶¶10-11; Ex. 32, Exhibit A ¶¶217-18; Ex. 10 at 122:5-15. For example, [redacted] Ex. 7 ¶¶14-16; Ex. 8 ¶6; Ex. 9 ¶¶10-11; Ex. 32, Exhibit A ¶¶217-18. Accordingly, because XMTT has no evidence that the cores "***execute***" (or even retire) instructions in serial, the Court should grant summary judgment of no literal infringement. *Cephalon, Inc. v. Watson Pharm., Inc.*, 707 F.3d 1330, 1340 (Fed. Cir. 2013).

Additionally, while XMTT's recent technical expert reports are silent on the plain meaning of "serial processor" and "serial processing mode," Dr. Conte asserted at his deposition that [redacted]

[redacted] Ex. 10 at 149:4-23, 180:14-19. But that late and unsupported assertion does not square with the plain meaning of the claim language, or XMTT's past admissions, and XMTT cannot now attempt to modify the claims through claim construction. XMTT has repeatedly asserted that the terms "serial processor" and "serial processing mode" do not require claim construction, *see, e.g.*, D.I. 224 at 4-5, 21; D.I. 265 at 7; D.I. 293 at 4. XMTT cannot backtrack and argue, without disclosure or support, that the plain and ordinary meaning is tied to a "serial program" and "expected results" that are untethered to the claims. *Microchip Tech. Inc. v. Aptiv Servs. US, LLC*, No. 1:17-cv-01194, 2022 WL 4119755, at *3 (D. Del. Sept. 9, 2022) (finding forfeiture of claim construction argument when the party did not request construction).

D. The accused Intel processors do not infringe under the doctrine of equivalents

XMTT asserts that the highly parallelized cores in the accused products are equivalent to the "serial processor" in the claims. That argument, however, vitiates the "serial processor" claim element. It also disregards the substantial differences that exist between the claimed "serial processor," which executes instructions one at a time, and the cores in the accused products, which are parallel at all stages of their pipelines. Intel's core architects have dedicated decades of research and substantial resources into improving performance by increasing the parallelism in the cores as much as possible, making them substantially different from serial processors.

1. XMTT's doctrine of equivalents theory would vitiate the "serial processor" claim element

The premise of XMTT's doctrine of equivalents theory is that, even if Intel's accused product cores are not literally serial processors—*i.e.*, even if they are parallel processors—they are equivalent to serial processors. But the asserted claims require ***both*** a "serial processor" and a "plurality of parallel processors" (*e.g.*, Ex. 4 at claim 1), and XMTT's doctrine of equivalents

argument vitiates the "serial processor" limitation by erasing the distinction between it and the separate "plurality of parallel processors" limitation. *See, e.g.*, *Iris Corp. Berhad v. United States*, 148 Fed. Cl. 173, 175 (2020) (finding vitiation where the doctrine of equivalents theory "collapses separate steps into one"). Said differently, XMTT is attempting to prove infringement of the asserted claims by eliminating the "serial processor" requirement and instead pointing to a "parallel processor" and a "plurality of parallel processors," which is prohibited by the vitiation doctrine. *See Akzo Nobel Coatings, Inc. v. Dow Chem. Co.*, 811 F.3d 1334, 1342 (Fed. Cir. 2016).

Moreover, under the "specific exclusion" principle—a corollary of the vitiation doctrine—the Federal Circuit has held that "the concept of equivalency cannot embrace a structure that is specifically excluded from the scope of its claims." *Dolly, Inc. v. Spalding & Evenflo Cos.*, 16 F.3d 394, 400 (Fed. Cir. 1994). Based on this principle, courts have "refused to apply the doctrine [of equivalents] in other cases where the accused device contained the antithesis of the claimed structure." *Planet Bingo, LLC v. GameTech Int'l, Inc.*, 472 F.3d 1338, 1345 (Fed. Cir. 2006); *see also MorphoSys AG v. Janssen Biotech, Inc.*, 358 F. Supp. 3d 354, 362 (D. Del. 2019) ("[T]he doctrine of equivalents cannot broaden a claim to cover a feature that is 'the opposite of, or inconsistent with, the recited limitation.'") (quoting *Augme Techs., Inc. v. Yahoo! Inc.*, 755 F.3d 1326, 1335 (Fed. Cir. 2014)).

The "specific exclusion" principle is frequently used to reject equivalence between two things that are opposites of each other. *Augme*, 755 F.3d at 1335 ("Because the Augme patents make clear that embedded and linked code are opposites, we agree with the district court that they cannot possess only insubstantial differences.") (quotations omitted); *SciMed Life Sys. v. Advanced Cardiovascular Sys.*, 242 F.3d 1337, 1347 (Fed. Cir. 2001) ("[I]f a patent states that the claimed device must be 'non-metallic,' the patentee cannot assert the patent against a metallic device on

the ground that a metallic device is equivalent to a non-metallic device."); *Moore U.S.A., Inc. v. Standard Register Co.*, 229 F.3d 1091, 1106 (Fed. Cir. 2000) ("[I]t would defy logic to conclude that a minority--the very antithesis of a majority--could be insubstantially different from a claim limitation requiring a majority, and no reasonable juror could find otherwise.").

Serial processors and parallel processors are fundamentally different from—and, in fact, are opposites of—each other. The terms "parallel" and "serial" are antithetical to each other because executing multiple instructions concurrently is the opposite of executing one instruction at a time. The patents confirm the binary nature of "serial" and "parallel" by using those terms in different limitations to describe different processors and different forms and modes of execution. Ex. 4, claims 1, 19, 33; Ex. 5, claims 1, 20. The specifications also consistently describe "serial" and "parallel" as opposites (Ex. 4 at 4:39-46), as do technical dictionaries from the time of the patents (Exs. 25; 26; 27; 28), and other patents and publications from Dr. Vishkin. Ex. 23 at 7:40-49; Ex. 29 at 2; Ex. 30 at 1; Ex. 31 at 2-3. And the asserted claims require ***both*** a "serial processor" and "parallel processors" to be present (Ex. 4, claims 1, 19, 33; Ex. 5, claims 1, 20), which further confirms that, as a matter of law, the two types of processors are different. *Helmsderfer*, 527 F.3d at 1382 ("different claim terms are presumed to have different meanings"). Accordingly, if something is a "parallel processor," it cannot also be a "serial processor" (nor vice versa). *See, e.g.*, *MorphoSys*, 358 F. Supp. 3d at 363 ("[G]iven that a human antibody cannot also be a humanized antibody (and vice versa), the terms are 'inconsistent with each other.'" (quoting *Augme*, 755 F.3d at 1335)). The "specific exclusion" doctrine thus prevents XMTT from using the doctrine of equivalents to stretch claims directed toward a "serial processor" to cover the accused core processors, which are indisputably parallel. *Augme*, 755 F.3d at 1335; *Planet Bingo*, 472 F.3d at 1345.

The Court should therefore grant summary judgment of no infringement under the doctrine of equivalents because XMTT's theory would vitiate the "serial processor" element by rendering it meaningless. *See Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29-30 (1997).

2. The accused cores do not perform the same function in the same way to achieve the same result as the claimed "serial processor"

XMTT also cannot show that the cores in the accused products perform the same function in the same way to achieve the same result as the "serial processor" recited in the claims. Dr. Conte sets forth a function-way-result analysis that relates entirely to whether [redacted] Ex. 6 ¶¶195-97. But Dr. Conte's analysis does not even attempt to show how a parallel processor that executes multiple instructions simultaneously in parallel is somehow equivalent (in function, in way, or in result) to a serial processor that executes instructions one at a time. *Id.* Under the function-way-result test, the cores in the accused products perform their *function* of executing instructions in parallel, by *way* of employing parallelism throughout the entire pipeline, to achieve *results* of higher performance than can be achieved with a serial processor, as shown by the undisputed facts discussed below. *See infra*, Section I.D.3. Therefore, XMTT cannot meet its burden to satisfy the function-way-result test under the doctrine of equivalents. *See MiiCs & Partners Am., Inc. v. Toshiba Corp.*, 282 F. Supp. 3d 844, 849–50 (D. Del. 2017) (granting partial summary judgment of no infringement by the doctrine of equivalents for failure to meet the function-way-result test).

3. The undisputed facts demonstrate that there are substantial differences between the accused Intel cores and the claimed "serial processors"

[4] The cores' out-of-order execution (Ex. 7 ¶¶17-20; Ex. 8 ¶7; Ex. 9 ¶¶12-14) is a separate and independent reason why they do not meet the "serial processor" limitation either literally or under the doctrine of equivalents (Ex. 32, Exhibit A ¶¶240-49, 265-67), and Intel may pursue that noninfringement theory if this case goes to trial.

"[C]ourts must consider the totality of the circumstances of each case and determine whether the alleged equivalent can be fairly characterized as an insubstantial change from the claimed subject matter without rendering the pertinent limitation meaningless." *Freedman Seating Co. v. Am. Seating Co.*, 420 F.3d 1350, 1359 (Fed. Cir. 2005). One important consideration is whether a difference is "a clear, substantial difference or difference in kind," rather than a "subtle difference in degree." *Id.* at 1361 (quoting *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 149 F.3d 1309, 1321 (Fed. Cir. 1998)). The Federal Circuit has noted it is "more difficult" to prove differences are insubstantial "when the accused structure has an element that is the opposite of the claimed element, especially where the specification or prosecution history highlights the differences." *Brilliant Instruments, Inc. v. GuideTech, LLC*, 707 F.3d 1342, 1347–48 (Fed. Cir. 2013); *Moore*, 229 F.3d at 1106. "If the claimed and accused elements are recognized by those of skill in the art to be opposing ways of doing something, they are likely not insubstantially different." *Id.*

The differences between "parallel" and "serial" processing are substantial because they are opposite ways of executing instructions. *See* Section I.A. Intel heavily invested its time and resources to move away from serial processing in its cores, and instead increase the amount of parallelism in each generation of its products. Ex. 7 ¶24; Ex. 8 ¶¶11-12; Ex. 9 ¶¶16-19. Intel's [redacted] Ex. 7 ¶24; Ex. 8 ¶¶11-12; Ex. 9 ¶¶16-19. For example, [redacted]

These increases in parallelism have come with significant costs and trade-offs. To achieve their improved performance, the cores require substantial amounts of hardware throughout their architectures that are dedicated to parallelism. The cores have parallel hardware units at the execution stage, including arithmetic logic units, and load/store units. Ex. 7 ¶¶12, 24; Ex. 8 ¶¶11-12; Ex. 9 ¶17. And they have parallel hardware units in other stages of their pipelines that are necessary to avoid bottlenecks and keep the parallel execution units consistently fed with multiple instructions to execute in parallel. Ex. 7 ¶¶14-16, 24; Ex. 8 ¶¶11-12; Ex. 9 ¶¶10, 17. Each core contains parallel decode units that decode multiple instructions simultaneously, as well as a Reorder Buffer (ROB) that retires multiple instructions in parallel after execution. Ex. 7 ¶¶14-16, 18; Ex. 8 ¶¶6-7; Ex. 9 ¶13. The ROB also tracks all "in-flight" instructions being processed simultaneously throughout the pipeline, and its size determines the number of in-flight instructions it can track—[redacted]. Ex. 7 ¶18; Ex. 8 ¶7; Ex. 9 ¶13.

Many of these additional hardware units and buffers that are dedicated to supporting parallelism in Intel's cores would be unnecessary if Intel used serial processors that issue and execute one instruction at a time. Ex. 7 ¶¶24-25; Ex. 8 ¶¶11-15; Ex. 9 ¶¶17-20. Accordingly, the cores are substantially different "in kind" from serial processors, *see Freedman Seating*, 420 F.3d at 1361, and the Court should grant summary judgment because XMTT cannot meet its burden to show equivalence. *See Sage Prods., Inc. v. Devon Indus., Inc.*, 126 F.3d 1420, 1423 (Fed. Cir.1997) ("[T]he trial court should grant summary judgment in any case where no reasonable fact finder could find equivalence.").

II. THE COURT SHOULD GRANT SUMMARY JUDGMENT OF NO PRE-SUIT WILLFUL INFRINGEMENT

Dr. Vishkin testified at his deposition that, [redacted]. Ex. 11 at

39:18-22, 96:3-13. "Knowledge of the asserted patent and evidence of infringement is necessary, but not sufficient, for a finding of willfulness." *Bayer Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 988 (Fed. Cir. 2021). "Willfulness necessarily involves knowledge of the patent ***and*** of infringement." *Evonik Degussa GmbH v. Materia, Inc.*, 305 F. Supp. 3d 563, 577 (D. Del. 2018) (emphasis in original). Because XMTT cannot show that Intel had knowledge of the patents or knowledge of infringement, the Court should grant summary judgment of no pre-suit willfulness.

A. Intel lacked knowledge of the '388 patent or the '879 patent

First, the Court should grant summary judgement of no pre-suit willful infringement because there is no genuine dispute that Intel lacked knowledge of the asserted patents until XMTT filed suit. *See Bayer*, 989 F.3d at 988. This is not a close call—Dr. Vishkin conceded multiple times that [redacted] Moreover, despite having access to [redacted], XMTT has not identified any evidence that Intel was aware of either asserted patent.

In its discovery responses, XMTT asserts knowledge based on Dr. Vishkin's communications with Intel (Ex. 36 at 2-6; *see also* Ex. 6 ¶¶526, 541-43, 550), but none of those

communications is sufficient to create a genuine dispute. Many of the alleged interactions occurred well before the asserted patents issued, *see id.*, and are insufficient to show knowledge of the patents as a matter of law. *See State Indus. v. A.O. Smith Corp.*, 751 F.2d 1226, 1236 (Fed. Cir. 1985) ("[T]o willfully infringe *a patent*, the patent must exist and one must have knowledge of it."); *NexStep, Inc. v. Comcast Cable Communs., LLC*, No. 19-1031, 2019 WL 5626647, at *3 (D. Del. Oct. 31, 2019) ("NexStep has failed to plausibly plead pre-suit knowledge of the patents-in-suit because, when Dr. Stepanian met with Comcast, none of the patents-in-suit had issued."). And Dr. Vishkin never notified Intel of the asserted patents after they issued—even when [redacted] Ex. 37 at 1. General discussions about Dr. Vishkin's XMT architecture are insufficient to show knowledge of the asserted patents as a matter of law. *See, e.g.*, *MONEC Holding AG v. Motorola Mobility, Inc.*, 897 F. Supp. 2d 225, 232–33 (D. Del. 2012) (finding participation in same technologically-based industry insufficient to establish knowledge of the patent); *VLSI Tech. LLC v. Intel Corp.*, No. 18-0966, 2020 WL 3488584, at *5 (D. Del. June 26, 2020) ("Allegations about monitoring competition generally and about patents not asserted here do not plausibly establish that Intel had knowledge of infringement of the #633 and #331 patents.").

The closest XMTT comes is [redacted] However, those circumstances are legally insufficient to show knowledge of the patent itself. *State Indus.*, 751 F.2d at 1236 ("Filing an application is no guarantee any patent will issue and a very substantial percentage of applications never result in

patents. What the scope of claims in patents that do issue will be is something totally unforeseeable."); *see also, e.g.*, *iFIT Inc. v. Peloton Interactive, Inc.*, No. 21-507, 2022 WL 609605, at *2 (D. Del. Jan. 28, 2022) ("Knowledge of a patent application alone, however, is not enough to establish knowledge of the patent(s) that issued from that application and therefore not enough to establish willfulness."). Moreover, [redacted] further undermining any claim that those communications could give rise to the willful infringement.

XMTT's assertions of willful blindness are likewise unsupported. Willful blindness requires (1) subjective belief of high probability that a fact exists and (2) deliberate actions to avoid learning the fact, *Global-Tech Appliances, Inc. v. SEB S.A.*, 563 U.S. 754, 769 (2011), but no evidence exists that anyone at Intel believed the asserted patents existed, yet took deliberate actions to avoid learning of them. To the contrary, [redacted]. Ex. 37 at 1.

B. Intel lacked knowledge of the alleged infringement

Second, the Court should grant summary judgement of no pre-suit willful infringement because there is no dispute that Intel did ***not*** have knowledge of the alleged infringement until XMTT filed suit. *See Bos. Sci. Corp. v. Nevro Corp.*, 560 F. Supp. 3d 837, 843 (D. Del. 2021) ("Knowledge of a patent is not the same thing as knowledge that a product or the use of that product infringes the patent."); *Evonik*, 305 F. Supp. 3d at 577 (finding willfulness requires knowledge of the patent "***and*** of infringement"). Again, Dr. Vishkin conceded that [redacted] Ex. 11 at 39:18-22, 96:3-13. Nor is there any evidence that any Intel employee believed the accused products infringed the asserted patents,

much less took steps to avoid learning about any alleged infringement, thus XMTT cannot show willful blindness regarding the alleged infringement. *Global-Tech*, 563 U.S. at 769.

To the contrary, the undisputed evidence shows that Dr. Vishkin repeatedly criticized the Intel architecture used in the accused products. For example, even before the patents issued, [redacted]. Exs. 13, 14. In 2014, during the period of alleged infringement, Dr. Vishkin published an article describing Intel's multi-core products—the same products accused in this case—as "broken" and distinguishing them from his XMT approach. Ex. 15 at 1; Ex. 12 at 362:3-63:2. In 2016 and 2017, Dr. Vishkin told Intel that [redacted] Ex. 16 at 2; Ex. 44 at 8.

Moreover, there is no evidence that Dr. Vishkin spoke to any person at Intel involved in developing the accused graphics architecture. XMTT's charges of willful infringement are tied to its garden-variety infringement theories, and thus insufficient to award enhanced damages for willful infringement. *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93, 109-10 (2016).

Simply put, there is no evidence that Intel had any knowledge of the alleged infringement before XMTT's lawsuit. To the contrary, Dr. Vishkin criticized Intel's products for ***not*** using his technology. The Court should thus grant summary judgment of no willful infringement.

III. THE COURT SHOULD EXCLUDE DR. SULLIVAN'S INCOME APPROACH

A. Dr. Sullivan's Regression Model And Damages Conclusions Are Not Tied To The Facts Of The Case

Dr. Sullivan's econometric regression model purports to measure the correlation between the number of EUs and an accused product's price. But Dr. Sullivan then bootstraps his alleged statistical ***correlation*** into damages conclusions that assume—without any evidence—that the addition of hypothetical additional EUs to a given processor ***causes or caused*** price increases for

Intel's accused products. That fundamental correlation-does-not-equal-causation mistake invalidates his entire damages theory. Moreover, even the statistical model purporting to determine a correlation between EUs and price fails, first, because Dr. Sullivan improperly treats EUs as a continuous variable when partial execution units ***cannot*** exist, and second, because EUs are strongly correlated with other variables in the model making it impossible to know how EUs ***alone*** are correlated with price. These problems, both individually and collectively, sever Dr. Sullivan's damages estimates from the facts of the case and warrant exclusion. *Exmark Mfg. Co. Inc. v. Briggs & Stratton Power Prod. Grp., LLC*, 879 F.3d 1332, 1349 (Fed. Cir. 2018) ("If the patentee fails to tie the theory to the facts of the case, the testimony must be excluded.").

1. Dr. Sullivan's Treatment Of Execution Units As A Continuous Variable Is Divorced From The Facts Of The Case

Dr. Sullivan's regression model uses the number of EUs, which are physical "stand-alone programmable computation unit[s]" used in graphics processing, as the parameter of interest. Ex. 6 ¶219 (quoting Intel's specification regarding "Execution Units (EUs)"). Yet, Dr. Sullivan introduces a critical flaw into his model when he treats EUs as a continuous variable (instead of a discrete variable), as if a processor could have a fraction of an EU. Ex. 17 ¶¶249, 251; Ex. 38 ¶203. But, incontrovertibly, a fraction of an EU is non-sensical, non-functional, and is not available in any real-world product. In fact, [redacted]. *See, e.g.*, Ex. 6 ¶136-37, 219. At best, Dr. Sullivan's model is measuring the value of a purely hypothetical feature, leading to an unscientific result that is untethered to the facts of this case. *See Uniloc USA, Inc. v. Microsoft Corp.*, 632 F.3d 1292, 1371 (Fed. Cir. 2011) ("Beginning from a fundamentally flawed premise and adjusting it based on legitimate considerations specific to the facts of the case nevertheless results in a fundamentally flawed conclusion.").

In his reply report, Dr. Sullivan attempts to justify his decision to recast a real-world hardware item as a continuous variable, protesting that if he were to account for the reality of discrete EUs, his approach could not quantify the patents' benefits: *See, e.g.,* Ex. 38 ¶¶203-04 ("Economic literature suggests that treating a variable as categorical rather than continuous can introduce multicollinearity[.]"). But that is no defense—if Dr. Sullivan must change facts to fit his regression model, that proves his model is not a reliable method for determining damages here. Regression models may be helpful in certain situations, but they "are only as good as the data and modeling efforts that go into them." *Stragent, LLC v. Intel Corp.*, No. 6:11-cv-421, 2014 WL 12611339, at *2 (E.D. Tex. Mar. 12, 2014) (Dyk, J.).

2. Dr. Sullivan's Regression Model Has A Fatal Multicollinearity Problem

Dr. Sullivan also ignores a fatal problem in his data—"multicollinearity"—which presents as strong correlations between his parameter of interest and other variables, making it impossible to isolate correlation between EUs and price. In his opening report, Dr. Sullivan chooses EUs as his "parameter of interest" and claims that his "regression analysis measures the effect that a change in execution units has on unit price of Intel products, ***holding constant all other explanatory variables***" (Ex. 17 ¶231), again mistaking correlation for causation. But after Dr. Perryman demonstrated through a correlation matrix and other tests that "Execution Units is strongly correlated" with numerous other variables (Ex. 39 ¶¶94-97), Dr. Sullivan neither attempted to correct his model nor disputed Dr. Perryman's correlation tests, but rather offered the handwaving assertion that "multicollinearity is not a concern for estimating the relationship between execution units and price in my model." Ex. 38 ¶¶181-82. However, multicollinearity is not merely a concern—it is a serious, fatal flaw in Dr. Sullivan's model, because the demonstrated, unrebutted, strong correlation between EUs and other variables makes it impossible to isolate the

purported correlation between the number of EUs and price, let alone that an increase in EUs ***causes*** a particular price effect. Therefore, Dr. Sullivan's results are riddled with error and not reflective of actual relationships between Intel's pricing and its processors' features.

Other courts have recognized that "a severe multicollinearity problem" in an expert's regression analysis "is fatal to the model":

> Multicollinearity problems typically arise when the independent variable is correlated with one of the control variables. If the control variables move together with the independent variable, it becomes impossible to isolate the effect of the independent variable on the dependent variable—which, after all, is the goal of regression analysis.

Reed Const. Data Inc. v. McGraw-Hill Companies, Inc., 49 F. Supp. 3d 385, 404 (S.D.N.Y. 2014), *aff'd,* 638 F. App'x 43 (2d Cir. 2016); *see also Stragent*, 2014 WL 12611339, at *2 (excluding regression model where "collinearity and multicollinearity bec[a]me issues," because "the analysis had to account for the fact that some features were always present together, making it difficult to determine what they contributed individually"). Indeed, Dr. Sullivan also recognizes that "[m]ulticollinearity occurs when independent variables in the regression are highly correlated," which "can cause imprecise estimation of regression coefficients." Ex. 17 ¶211 n.527 (citing the Federal Judicial Center's *Reference Guide on Multiple Regressions* (Ex. 40 at 324) ("The greater the multicollinearity between two variables, the less precise are the estimates of individual regression parameters, and an expert is less able to distinguish among competing explanations for the movement in the outcome variable.")).

Despite acknowledging the valid "concern" with multicollinearity in regression models, Dr. Sullivan never tested the results of his model to confirm that multicollinearity had not impacted his estimates. In response to Dr. Perryman's correlation tests identifying the strong correlation between EUs and other variables (Ex. 39 ¶¶94-97), Dr. Sullivan offers three excuses purporting to explain why multicollinearity is suddenly no longer "a concern for estimating the relationship

between execution units and price in [his] model." Ex. 38 ¶181-82. All three arguments are red herrings or completely contradicted by his own statements.

First, Dr. Sullivan asserts that correlation between regressors ***other than the variable of interest*** does not matter. *See id.* ¶181 ("If β1 is the parameter of interest, we do not really care about the amount of correlation between x2 and x3.") (citation omitted); *see also id*. ¶182; Ex. 41 at 271:22-272:3 ("It is established that multicollinearity among control factors, ***separate and apart from the variable of interest***, is not an issue for a valuation of the coefficient on the variable of interest."). That argument is inapplicable, because the undisputed results of Dr. Perryman's correlation tests demonstrate that Dr. Sullivan's chosen ***parameter of interest*** (EUs) is, in fact, "strongly correlated" with other variables. Ex. 39 ¶¶94-97.

Second, Dr. Sullivan again deflects by conflating multicollinearity with perfect collinearity. Ex. 38 ¶181 ("Multicollinearity only invalidates assumptions of ordinary least squares regression when two or more independent variables are perfectly collinear."). That is another red herring. Both perfect collinearity (100% overlap between variables) ***and*** multicollinearity (*i.e.*, strong, but not perfect collinearity) can render a model meaningless through an inability to isolate the effect of the independent variable on the dependent variable. *See* Ex. 40 at 324. Dr. Sullivan cannot simply brush aside the significant multicollinearity identified by Dr. Perryman, and his failure to address that flaw in his model renders his conclusions unreliable. *See, e.g.*, *In re REMEC Inc. Securities Litig.*, 702 F. Supp. 2d 1202, 1273 (S.D. Cal. 2010) (excluding expert who does not "test his model for multicollinearity").

Third, Dr. Sullivan appears to assert that multicollinearity is not a concern here because it is a problem "that arises with small data samples" and that his "regression analysis relies on approximately [redacted] observations." Ex. 38 ¶181. But at his deposition, Dr. Sullivan

acknowledged that "[o]ne can run improper analyses with a lot of data." Ex. 41 at 270:5-6. In fact, as Dr. Sullivan's own cited references confirm, a large data set does not protect against the perils of multicollinearity. *See* Ex. 40 at 325 ("[E]ven a large sample with substantial multicollinearity, may not provide sufficient information for the expert to determine whether there is a relationship."). Thus, this excuse cannot save his flawed analysis.

Accordingly, the significant multicollinearity in Dr. Sullivan's regression model means that the model's results are utterly unreliable. It is impossible to determine if his observed price relationship is attributable solely to the number of EUs, as opposed to its correlated variables. Yet, "the burden of proving helpfulness and relevance rests on the proponent of a regression analysis." *In re REMEC*, 702 F. Supp. 2d at 1273. Because XMTT cannot meet that burden, Dr. Sullivan's income approach regression model should be excluded.

B. Dr. Sullivan's Income Approach Fails To Apportion For The Value Of The Patented Improvement Over The Conventional Elements

Dr. Sullivan's regression analysis is also flawed and contrary to law because his analysis attempts to calculate damages based entirely on conventional features in the accused Intel products: (1) the graphics L3 cache (which XMTT contends is the claimed "partitioned memory modules") and (2) the sampler cache (which XMTT contends is the claimed "read-only memory"). Ex. 17 ¶¶97-100. But it is black-letter law that a patentee cannot calculate damages based on the use of conventional, well-known components, even if they are recited in the claims. *See, e.g.*, *Exmark*, 879 F.3d at 1348 (holding that the "patent owner must apportion or separate the damages between the patented improvement and the conventional components of the multicomponent product"); *Omega Pats., LLC v. CalAmp Corp.*, 13 F.4th 1361, 1377 (Fed. Cir. 2021) ("[E]ven if the [accused products] have the same components as those set forth in the asserted claims, [patentee] still must adequately and reliably apportion between the improved and conventional

features of the accused [product] when using the [accused products] as a royalty base."). Dr. Sullivan ignores this fundamental principle and makes no attempt to measure the benefits of any alleged patented improvement. Instead, he values the impact of conventional components. Accordingly, his results are irrelevant to any damages owed to XMTT and must be excluded.

There is no dispute that the components that Dr. Sullivan measured are conventional. First, with respect to the '388 patent, the claimed component, "partitioned memory modules," was admittedly "well-known" in the art as of the time of the alleged invention. *See, e.g.*, Ex. 10 at 51:4-11 (admitting "partitioned memory modules were well-known concepts as of 2003"), 58:24-59:19, 63:25-64:10 (agreeing partitioning memory by address into a number of modules was an "established concept"). Similarly, level 3 caches—the accused components in Intel's processors—also were well-known in art. *See, e.g.*, Ex. 11 at 159:5-160:4 (Vishkin admitting he did not invent "level three caches"). Second, the '879 patent's claimed component, "read-only memory," was also well-known in the art as of the time of the alleged invention (at least as that term is applied by XMTT to include read-only caches). Indeed, the U.S. Patent Office recognized that "read-only caches" were "well-known in the art" during prosecution of the '879 patent. Ex. 42 at -323. Similarly, sampler caches—the accused components—also were well-known in the art. *See, e.g.*, Ex. 10 at 201:9-17 (admitting Intel's prior art graphics included a sampler cache).

The law requires that "the patent holder should only be compensated for the approximate incremental benefit derived from his invention." *Ericsson*, 773 F.3d at 1233. Dr. Sullivan ignored that requirement when he chose to measure the value of either disabling conventional caches (Dr. Annavaram's approach) or redesigning conventional caches (Dr. Conte's approach); both approaches value components that Dr. Vishkin ***did not invent***. If a patent claimed a car with (1) an improved gear selector plus (2) a conventional six-cylinder engine, it would be nonsensical to

attribute to the patent any performance gained by modifying the engine—any measured benefits would only reflect the prior art and would have nothing to do with the value of the invention. And that is all Dr. Sullivan's analysis does: measure the benefits of well-known, prior art components.

Additionally, Dr. Sullivan's reliance on XMTT's technical experts' inputs is further flawed because they each test ***different*** non-infringing alternatives for both patents, which leads Dr. Sullivan to inconsistent results. While Dr. Conte ***modifies*** the components in the accused products to measure die area savings, Dr. Annavaram completely ***disables*** them to measure performance improvement. *Compare* Ex. 6 ¶¶443-44 *with* Ex. 18 ¶¶37-38, 44, 51. Notably, Dr. Conte testified that [redacted] Ex. 10 at 211:17-22, 212:16-213:2. Even Dr. Sullivan agrees that his income approach results in [redacted]. Ex. 41 at 282:12-17; *see* Ex. 38 ¶10. For example, the approximate royalty for the '388 patent using die area savings benefits [redacted] Ex. 38 ¶10. And the royalty for the '879 patent using performance improvement benefits is [redacted]. *Id.* The Supreme Court advises that a standard for "reliability" is: "does application of the principle produce consistent results?" *Daubert v. Merrell Dow Pharmaceuticals, Inc.*, 509 U.S. 579, 590 n.9 (1993). Dr. Sullivan's approach fails that test.

Accordingly, Dr. Sullivan's income approach should be excluded, because his analysis of conventional components is irrelevant and his inconsistent results are unreliable.

C. Dr. Sullivan's Income Approach Awards XMTT 100% Of Intel's Profits

Even if Dr. Sullivan were able to correctly determine incremental revenue from his regression model, his purported "profit-split" analysis, where he awards 100% of Intel's

incremental profit to XMTT, disregards the parties' bargaining positions at the hypothetical negotiation. Dr. Sullivan ignores the real-world fact that Intel would never have implemented the patented invention if it would be left with no additional profit as a result, thus, his opinion is contrary to "rudimentary economics and common sense." *Looksmart Grp, Inc. v. Microsoft Corp.*, No. 17-cv-04709, 2019 WL 4009263, at *3 (N.D. Cal. Aug. 5, 2019). Just as the Federal Circuit rejected the "25% rule of thumb" in *Uniloc* and the "50-50 starting point" in *Virnetx*, this Court should exclude Dr. Sullivan's 100%-0% incremental "profit split" because it is "insufficiently grounded in the specific facts of the case." *Virnetx, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1331 (Fed. Cir. 2014); *Uniloc USA, Inc. v. Microsoft Corp.*, 632 F.3d 1292, 1318 (Fed. Cir. 2011).

Dr. Sullivan purports to deduct "incremental costs" (amounting to nothing more than added [redacted]) from "incremental revenue" to obtain what he calls "incremental profit"—even though that so-called "profit" does not account for [redacted] costs. Dr. Sullivan then, in what he calls a "contribution apportionment" step, removes [redacted] costs and awards the remainder—the entire profit allegedly derived from the patented technology—as a royalty to XMTT. Ex. 17 ¶¶310-24, 330-35 & Attachments I-1, K-1. In short, both steps of Dr. Sullivan's analysis deduct Intel's costs and he never divides the remaining profit between Intel and XMTT; instead, he awards the ***entire profit*** allegedly derived from the patented technology to XMTT, leaving Intel with nothing more than it would have obtained had it sold the accused products without the alleged invention. But Dr. Sullivan cites no evidence that his "profit-split" reflects Intel's hypothetical bargaining position or its real-world practice. That is because Dr. Sullivan's approach does not make economic sense; Intel would not bargain away 100% of the profit allegedly derived from the accused technology.

Applying the Federal Circuit's reasoning in *Virnetx*, courts have rejected damages theories that award 100% of the incremental profits to the patentee. In *Contour IP*, the Court held that "it would be unreasonable and unreliable for [the expert] to conclude that 100% of profits associated with the infringing technology would go to [the patentee]," because the accused infringer "was the maker, designer, marketer, seller, and undisputed market leader" and, notably, "***would not have left a hypothetical negotiation with zero profits derived from the infringing technology***." *Contour IP Holding, LLC v. GoPro, Inc.*, No. 3:17-cv-04738, 2020 WL 5106845, at *14 (N.D. Cal. Aug. 31, 2020). Similarly, in *Looksmart*, the Court held that "[a]s a matter of both rudimentary economics and common sense," the assumption that Microsoft would bargain away 100% of its cost savings is "insupportable" under the hypothetical negotiation framework:

> If Microsoft were required to pay a royalty consisting of all its avoided costs in order to use an invention, ***what would be the point of the invention?*** Microsoft would gain nothing by its use, so the hypothetical negotiation would never take place. Because Microsoft would be no better off by bargaining away all of its avoided costs, 100 percent of those costs cannot possibly be the royalty upon which the parties would have agreed [in a hypothetical negotiation]."

Looksmart, 2019 WL 4009263, at *3 (noting cost savings should be treated no differently than incremental profits) (internal citations and quotation marks omitted).

Ultimately, Dr. Sullivan assumed without any analysis that Intel would have bargained to recoup only its costs and allowed XMTT to walk away with all profits attributable to the patented invention, despite Intel's commercialization efforts. This has no basis in law or fact. Accordingly, Dr. Sullivan's income approach should be excluded.

IV. THE COURT SHOULD EXCLUDE DR. ANNAVARAM'S GRAPHICS PERFORMANCE OPINIONS

A. Dr. Annavaram's Equivalence Theory Is Divorced From The Facts

Dr. Annavaram conducted performance testing on a number of alleged non-infringing alternatives, then converted one hand-picked result from that testing—a performance benefit

supposedly attributable to the patented invention—into an increase in "execution units" so that Dr. Sullivan could use it as an input to his regression-based damages model. Dr. Annavaram, however, bases his conversion of "performance" to "execution units" on a fundamentally flawed assertion: that an increase in performance is "equivalent" to increase in EUs. Yet that assertion is based on a logical leap that is divorced from the facts of the case and unreliable. *See, e.g.*, *In re Lincoln Nat'l COI Litig.*, No. 16-6605, 2022 WL 4091220, at *7 (E.D. Pa. Aug. 9, 2022) ("[E]xpert opinions based on 'leaps of logic' and speculation are not reliable. Those unsupported assumptions also deprive [the expert] of the capacity to assist the finder of fact.") (citing *UGI Sunbury LLC v. A Perm. Easm. For 1.7575 Acres*, 949 F.3d 825, 835 (3d Cir. 2020)). In fact, Dr. Annavaram's assertion of equivalence is contradicted by both sets of graphics performance tests addressed in his report—one conducted by Dr. Annavaram as well as one found in an Intel internal document.

First, Dr. Annavaram's conclusion regarding the supposed "equivalence" between his measurement of "performance improvement" and number of EUs (required by Dr. Sullivan's convoluted damages theory) is inconsistent with the evidence on which it is based—[redacted] Ex. 18 ¶¶ 59-62. Dr. Annavaram's analysis of Intel data does not show "equivalence," as he asserts (*id.* ¶ 59); rather, he himself concludes that the data shows they are ***not*** equivalent—"[redacted]." *Id.* ¶61. Moreover, at his deposition, Dr. Annavaram confirmed that there is [redacted]. *See* Ex. 20 at 214:19-215:12 [redacted] 216:13-24 [redacted] Dr. Annavaram argues that he equates the EUs to performance to "be more conservative" (Ex. 18

¶62), but the law does not allow Dr. Annavaram to hide the lack of any basis for his assertion by simply calling his analysis "conservative." *Ayers v. Robinson,* 887 F. Supp. 1049, 1060 (N.D. Ill. 1995) ("[A] conservative opinion . . . does not equate to a scientific one."). Moreover, [redacted] itself has no bearing on the testing that Dr. Annavaram performed. The [redacted] on which he relies measured performance using a different metric ([redacted]) and a different benchmark (3DMark) than Dr. Annavaram's own testing [redacted]. *See* Ex. 18 ¶¶25, 53; Ex. 20 at 201:4-10 (admitting to not measuring the impact of execution units on his benchmark). And Dr. Annavaram does not explain how a document using completely different performance data and benchmark can support drawing conclusions about his testing, let alone how performance across [redacted] which also supports exclusion. *Gen. Elec. Co. v. Joiner*, 522 U.S. 136, 146 (1997) ("A court may conclude that there is simply too great an analytical gap between the data and the opinion proffered.").

Second, Dr. Annavaram's own test results show there is no equivalence between the number of EUs and performance, because they include dramatically different performance results for systems with the same number of EUs. For example, [redacted] Dr. Annavaram provides no excuse in his

report for ignoring the fact that his own data shows that there is no equivalence between EUs and performance.[5] At his deposition, Dr. Annavaram attempted to argue that the systems were "different graphics systems" (*see* Ex. 20 at 239:1-242:11), but that does not make sense, because Dr. Annavaram assumed less similar systems were "[redacted]. *See, e.g.*, Ex. 18 ¶61 ([redacted] Simply put, Dr. Annavaram's own testing shows no equivalence between EUs and performance and further demonstrates that his conclusion of "equivalence" is unfounded speculation.

In essence, the foundation for Dr. Annavaram's opinions on "converting performance measurements to equivalent hardware change" is [redacted] that does not show any such equivalence. Yet his threadbare and illogical conjecture is then used by Dr. Sullivan to support a [redacted] damages theory. Ex. 17 ¶¶21-22, 291-93. This is "the type of 'junk science' that a Daubert inquiry is designed to screen." *In re Intel Corp. Microprocessor Antitrust Litig.*, No. 05-1717, 05-485, 2010 WL 8591815, at *16 (D. Del. July 28, 2010).

B. Dr. Annavaram's Analysis Double-Counts The Impact Of The Patents

Dr. Annavaram's graphics performance testing also double-counts the supposed benefit of the asserted patents because he improperly adds the supposed "performance impacts" of removing two different components of the accused products—the L3 graphics cache and the L2 sampler

[5] Dr. Annavaram's analysis repeatedly disregards inconvenient testing results—he also cherry-picks testing results from one computer system as a supposed "[redacted]." Ex. 18 ¶57. In fact, Dr. Annavaram tested fifteen systems, but his testing results do not show any consistent "performance benefits" for either patent. Instead, Dr. Annavaram unscientifically chose to combine the benefits for both patents and pick as his [redacted] *Id.*. Ironically, Dr. Annavaram then reports to Dr. Sullivan his "conservative" results on a per-patent basis (Ex. 17 ¶¶291, 297) even though his tests show that several systems had significantly lower ***per-patent*** benefits. Ex. 18 ¶56.

cache—even though removing just one (the L3 graphics cache) would avoid infringement of ***both*** patents. There is no dispute that XMTT's infringement allegations depend on the L3 graphics cache for ***both*** the '388 and '879 patents. Ex. 6 ¶¶233-237 (asserting that the L3 graphics cache is the claimed "partitioned memory modules"), ¶¶397-400 (asserting that the L3 graphics cache is the claimed "shared memory modules"). Nonetheless, Dr. Annavaram performs two ***different*** tests for the '388 patent and '879 patent—disabling the L3 graphics cache to avoid infringement of the '388 patent and disabling the L2 sampler cache to avoid infringement of the '879 patent. *See* Ex. 18 ¶51, 56-57. Dr. Annavaram then ***adds*** both of these "performance improvements" to obtain an alleged [redacted] *See id.* ¶57. But Dr. Annavaram's "addition" of the two results is both unsupported and illogical—if infringement could be avoided with only a [redacted] impact to "performance" by disabling the L3 cache, there would be no reason to also disable the L2 sampler cache and take another purported hit to performance. At his deposition, Dr. Annavaram had no explanation for why Intel would remove two components to avoid infringement if one would do. Ex. 20 at 248:5-249:13. Nor does Dr. Sullivan explain why Intel would value the two patents separately when removing one component would resolve infringement of both. Accordingly, Intel requests that the Court exclude Dr. Annavaram's additive "performance benefit" calculations for the '879 patent.

CONCLUSION

For the foregoing reasons, Intel respectfully requests that this Court grant Intel's motions for summary judgment of noninfringement and no pre-suit willfulness and also exclude Dr. Sullivan's income approach opinions and Dr. Annavaram's graphics performance opinions.

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CERTIFICATE OF SERVICE

I hereby certify that on December 22, 2022, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF, which will send notification of such filing to all registered participants.

I further certify that I caused copies of the foregoing document to be served December 22, 2022, upon the following in the manner indicated:

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